Curriculum Vitae – Prof. David ATIENZA ALONSO

1. CONTACT INFORMATION

Position:	Assistant Professor (Tenure-Track) and Director of the Embedded Systems Laboratory (ESL)
Affiliation:	Institute of Electrical Engineering, Faculty of Engineering (STI), Ecole Polytechnique Fédérale de Lausanne (EPFL)
Mail address:	EPFL-STI-IEL-ESL, Station 11 1015-Lausanne (Switzerland)
Phone:	(+41) (0) 21-693-11-31
Fax:	(+41) (0) 21-693-11-30

2. LANGUAGES

Spanish: native speaker; English: fluent; French: fluent; German: basic knowledge

3. RESEARCH INTERESTS

My research interests focus on system-level co-design (HW/SW) methodologies and design automation for high-performance embedded systems and low-power *Systems-on-Chip (SoC)*, with particular emphasis on novel thermal- and reliability-aware design methods for 2D/3D *Multi-Processors System-on-Chip (MPSoCs)*, dynamic memory management and memory hierarchy optimizations for embedded systems, and flexible interconnection paradigms (*Networks-on-Chip or NoCs*) for deep sub-micron integrated circuits. Also, my research interests cover performance and low-power optimizations in the operating system middleware, memory hierarchy and processing architectures (i.e., microcontrollers, digital signal processors or very-long instruction word architectures) of *Wireless Body Sensor Networks (WBSN)* to perform biomedical monitoring, as well as the application of energy scavenging mechanisms to power up these WBSNs for longer and more reliable operation.

4. EDUCATION

Jun. 2005	PhD in Computer and Systems Engineering with European Degree as sandwich PhD student between the Inter-University Micro-Electronics Center (IMEC) vzw, Leuven (Belgium) and Complutense University of Madrid (Spain). Average Grade: summa cum laude (4.0 GPA), Thesis: *"Multi-level Methodology for the Refinement of the Dynamic Memory Subsystem in Dynamic Multimedia Embedded Systems"* (only fully available in Spanish).
Jun. 2001	M.Sc. in Computer Engineering, Complutense University of Madrid (UCM). Graduation project: "Virtual building: 3-D web-based recreation of a Computer Science Faculty". Average Grade: 9/10.
Jun. 1999	B.Sc. in Computer Engineering, UCM. Average grade: summa cum laude.

5. ACADEMIC POSITIONS

Since Oct. 2008	Assistant Professor (Tenure-Track) of Electrical Engineering and Director of the Embedded Systems Laboratory (ESL) at Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, VD, Switzerland. Adjunct Professor of Computer and Systems Engineering at Complutense University of Madrid (UCM), Spain.
Apr. 2007 – Sept. 2008	Associate Professor in the Department of Computer Architecture and Systems Automation (DACYA) of the UCM, Spain.
Mar. 2007	"*Habilitation*" (venia docendi) in CS and CE from the Tenure-Level National Evaluation Committee in Spain, right to be appointed as Associate Professor in any university in Spain.
Jul. 2005 – Apr. 2007	Senior Research Associate in the Integrated Systems Laboratory (LSI) of Prof. Giovanni De Micheli in Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, VD, Switzerland.
Oct. 2005 – Mar. 2007	Part-Time Assistant Professor in the Department of Computer Architecture and Automation of the UCM, Spain
Jan.2002 - Jun. 2005	Research Assistant and PhD Student at the Design Technology (DDT) Group of IMEC vzw, Leuven, Belgium.
Sep. 2001 – Jun. 2005	Teaching Assistant and PhD Student at the Department of Computer Architecture and Automation, UCM, Spain.
Sep. 2000 – Jun. 2001	Research Fellow within the Computer Science Faculty of UCM for developing the project entitled: "VHDL code-to-code transformation for improving HW conditional reuse".

6. AWARDS AND SCHOLARSHIPS

2012 Recipient of the **ACM Outstanding New Faculty Award (ONFA)**, given by the ACM Interest Group on Design Automation (SIGDA) for the "demonstrated great potential as a lead researcher and educator in the field of electronic design automation".

2011 **Outstanding External Research Award** by Oracle-Sun Microsystems Labs. ($150K donation) for contributions to the area of "Global Thermal and Energy-Aware Feedback-Control Algorithms for Enterprise Computer Servers".

2010 **Best Paper Award Nomination** – IEEE/ACM International Conference on High Performance Computing & Simulation (HPCS'10).

2009 **Best Paper Award** 17th IEEE/IFIP Very Large Scale Integration Conference (VLSI-SoC'09).

2007 **IBM Innovative Project Award,** "Optimization of Dynamic Memory Allocation in Embedded Systems Using Evolutionary Computation", 5th Certamen Arquímedes 2007, Ministry of Education and Science, Spain.

2006 **Best Paper Award Nomination** - System-Level Design Tools Track, IEEE International Conference on Computer-Aided Design (ICCAD'06).

2004 **Best Paper Award Nomination** - CAD and Tools Track, ACM/IEEE Design Automation Conference (DAC'04).

2002 – 2004 **Early-Stage European Marie Curie Research Grant**, European Commission, Brussels, Belgium.

2000 – 2001 National Research Scholarship, granted by the Ministry of Research & Education, Spain.

7. RESEARCH GRANTS AND PROJECTS

03/2012-01/2013 Advanced Research Grant from Nokia Corporation: "Multimodality Sensing Platforms Design". **(PI, Total budget: 165K EUR)**.

06/2011-05/2012 **Deputy Director for EPFL of European Commission (EC) FET Flagship Project**: "Guardian Angels", in cooperation with 25 industrial and academic partners in Europe. **(Tentative target Budget: 1B EUR (100M EUR x 10 years); Pilot Project phase funding: 2.5M EUR).**

01/2011-12/2015 Advanced Research Grant from Centre Suisse d'Electronique et de Microtechnique (CSEM): "Energy-Aware Compilation Techniques for High-Performance Embedded Processing Architectures". **(PI, Total budget: 220K EUR)**.

01/2011-12/2012 Advanced Silicon SA, Research Grant: "System-Level Design of Advanced 3D Touch Screen Interfaces for Smartphone and High-Performance Embedded Systems" **(PI, Total budget: 180K EUR)**.

01/2011-12/2012 Credit Suisse - IT Development Center at Parc Scientifique, Industrial research project grant: "Smart data center monitoring: a thermal-aware design approach to Green IT" to improve the energy monitoring visibility and thermal-aware design of Credit Suisse datacenter infrastructures. **(PI, Total budget: 180K EUR)**.

10/2010-05/2011 Co-Investigator and Host Center of two FP7 visiting researchers grant: "EU FP7 European NoE on High-Performance Embedded Architectures and Compilation (HiPEAC-2)", European Commission FP7 - ICT Networks of Excellence, in cooperation with Politecnico di Milano.

10/2010-09/2014 Long-Term Research Grant from Inter-University Micro-Electronics Center (IMEC): "On-Line Process Variation and Reliability Compensation for Dynamic Systems with Hard Constraints and Proactive Control Techniques". **(PI, Total budget: 390K EUR)**.

05/2010-04/2011 Nano-Tera – Focused Research (NTF) Project: "BioCS-Node: Enabling Ultra-Low-Power Ambulatory Monitoring of Cardiac and Neurological Bioelectrical Signals Using Compressed Sensing", in cooperation with LTS2-EPFL (CH). **(Total Budget: 180K EUR; Co-PI funding: 100K EUR)**.

04/2010-03/2012 Swiss NSF Research Project (Div. II):"Scalable High-Performance Computing Simulator for Manycore Platforms". **(PI, Total budget: 380K EUR)**

02/2010-01/2013 Swiss NSF Research Project (Div. II):"Dynamically Adaptive Architectures for Nomadic Embedded Systems", in cooperation with Politecnico di Milano (IT). **(PI, Total budget: 310K EUR)**.

01/2010-12/2012 **European Commission FP7 ICT-Call 4 – 3.6 Computing Systems, STREP Project**: "PRO3D: Programming for Future 3D Architectures with Many Cores", in cooperation with CEA-LETI (FR), ST Microelectronics (FR), Verimag (FR), Univ. of Bologna (IT), TIK-ETHZ (CH). **(Total Budget: 2.7M EUR; Co-PI funding: 470K EUR)**.

09/2009–09/2013 Long-Term Research Framework between Nestlé and EPFL: "Smart Embedded Systems Design and Wearable Technologies Development for Healthy-Life Wireless Body Area Networks Monitoring" **(PI, Total Budget: 540K EUR)**.

06/2009-12/2013 Nano-Tera – Cooperative Research (RTD) Project: "CMOSAIC: 3D Stacked Architectures with Interlayer Cooling", in cooperation with LTCM and LSM-EPFL (CH), IBM Zürich (CH), LTNT and FML-ETHZ (CH). **(Total Budget: 2.1M EUR; Co-PI funding: 310K EUR)**.

10/2007–01/2009 Principal Investigator of the industrial project "Software Techniques for the Analysis of Radio Signals Obtained with Automatic Captures Using Embedded Systems", between UCM, Spain, and Indra Systems, Spain. **(PI, Total Budget: 45K EUR)**.

01/2007-01/2012 Scientific Counselor of long-time research at the Holst Stitching IMEC-NL Research Center, Eindhoven, Holland.

01/2006–12/2008 Scientific Group Coordinator in the project "Materials, Devices and Design Technologies for Nanoelectronic Systems Beyond 22 nm CMOS", granted by Swiss Competence Center for Material Science and Technology (CCMX), Switzerland. **(Total Budget: 1.3M EUR; Co-PI funding: 290K EUR)**.

10/2005–09/2010 Principal Investigator of the project "Compilers, Dynamic Memory Management and Storage Exploration", between UCM, Spain, and Holst Stitching IMEC-NL Research Center, Eindhoven, Holland. **(PI, Total Budget: 140K EUR)**.

05/2005–12/2007 Scientific Coordinator for UCM of EU FP6 European Network of Excellence on High-Performance Embedded Architectures and Compilers (HiPEAC), European Commission.

07/2005–06/2006 Scientific Counselor of long-time research at the Digital Design Technology (DDT) Group of Inter-University Micro-Electronics Center (IMEC), Leuven, Belgium.

01/2005-12/2005 Sub-Project Coordinator in the project "HW/SW Technology for High-Performance Systems" granted by the Spanish Government (CYCIT, TIC 2002/0750).

06/2003–05/2005 Internal Project Coordinator for IMEC of EU FP6 project "Multi-Layer Memory Management for Low Power Embedded Systems", European Commission, Marie Curie Actions.

8. PROFESSIONAL ACTIVITIES

8.1 Conference Organization

- Preselected as Technical Program Chair of the ACM/IEEE Design Automation and Test in Europe Conference (DATE) in 2014.
- "Application Design" Track Chair of the ACM/IEEE Design Automation and Test in Europe Conference (DATE) in 2012 (and appointed for 2013).
- General Chair of the ACM 21st Great Lakes Symposium on VLSI (GLSVLSI), in 2011.
- Executive Committee Member of the ACM/IEEE Design Automation and Test in Europe conference (DATE), since 2010.
- General Chair: IEEE/IFIP 18th Very Large Scale Integration and System-on-Chip (VLSI-SoC) Conference in 2010.
- General Chair of the IEEE 2nd Design for 3D Integration Workshop (D43D) in 2010.
- Technical Program Chair ACM 20th Great Lakes Symposium on VLSI (GLSVLSI) in 2010.
- Topic Chair: ACM/IEEE Asian Pacific Design Automation Conference (ASP-DAC), 2012. ACM/IEEE Design Automation and Test in Europe (DATE) Conference, 2010-2011; ACM/IEEE International Conference on Computer-Aided Design (ICCAD), in 2009.
- Publicity Co-Chair: IEEE International Symposium on VLSI (ISVLSI) 2009; ACM Great Lakes Symposium on VLSI (GLSVLSI), 2009; IEEE/IFIP VLSI-SoC Conference, in 2008.
- Session Chair: IEEE/ACM Design Automation and Test in Europe (DATE) Conference, 2006 – 2010; ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2006 - 2008.
- Program Co-Chair of the Symposium "Efficient Network-on-Chip implementation/emulation techniques for System-on-Chip design exploration", co-

located with Parallel Computing (ParCo) Conference, 2005.

- Local Committee Organizer 10th IEEE International Symposium on High Performance Computer Architecture (HPCA-10) 2004.

8.2 Committees

- Vice-President of Conferences and Technical Activities of the IEEE Council on Electronic Design Automation (CEDA), period 2012-2013.
- Elected Officer of the Board of Governors of the IEEE Circuits and Systems (CAS) Society, period 2010-2014.
- Vice-President of Finance of the IEEE Council on Electronic Design Automation (CEDA), period 2010-2011.
- Elected Executive Committee Officer of the IEEE Council on Electronic Design Automation (CEDA), period 2008 – 2009.
- Member of the Technical Programme Committee (TPC) of the ACM/IEEE International Symposium on System Synthesis and Codesign of Embedded Systems (CODES+ISSS), part of the Embedded Systems Week (ESWEEK), since 2012.
- Member of the TPC of the IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC) since 2008.
- Member of the TPC of the joint IEEE 22nd International Conference on VLSI Design and 8th Int. Conf. on Embedded Systems (VLSI and ES Design) since 2008.
- Member of the TPC of the IEEE Symposium on Integrated Circuits and System Design (SBBCI) since 2007.
- Member of the TPC of the IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS) since 2007.
- Member of the TPC of the International workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) since 2007.
- Member of the TPC of the ACM Great Lakes Symposium on VLSI (GLSVLSI) since 2007.
- Member of the TPC of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), period 2006-2008.
- Member of the TPC of the IEEE/ACM Design Automation and Test in Europe (DATE) Conference since 2006.
- Member of the Council of the School of Computer and Communication Sciences, EPFL, as representative of the Intermediary Body, period February 2006 – September 2008.
- Member of the Administrative and Advisory Boards of Marie Curie Fellowship Association from the European Commission from 2003 to 2005

8.3 Editorial Work

- Associate Editor of IEEE Transactions on Computer-Aided Design (T-CAD), period 2008-2014.
- Associate Editor of IEEE Letters on Embedded Systems (ES-L), period 2009-2012.
- Associate Editor of Elsevier Integration – The VLSI Journal, period 2008-2014.

8.4 Reviewer

- Expert Reviewer of FP7 Collaborative Projects for the European Commission, since 2011.
- Expert Evaluator of National Research Projects (TEC, National Plan I+D+i) for the Ministry of Research and Innovation in Spain, since 2011.
- ACM Transactions on Design Automation for Embedded Systems (TODAES) journal,

since 2007; IEEE Design and Test of Computers (D&T) Magazine, since 2008; Elsevier Journal of Parallel and Distributed Computing (JPDC), since 2007; IEEE Circuits and Systems Magazine, since 2007; Hindawi Journal on VLSI Design, since 2005; IET Computers & Digital Techniques, since 2005; IEEE Transactions on VLSI Systems (T-VLSI) journal, since 2005; ACM Transactions on Embedded Computing Systems (TECS) journal, since 2005; IEEE Transactions on Computer-Aided Design (T-CAD), period 2005 – 2007; Elsevier Microprocessors & Microsystems, since 2005; Computer Magazine - IEEE Computer Society, since 2004.

- IEEE International Conference on Circuits and Electronic Systems (ICECS), since 2007; IEEE International Symposium on Networks-on-Chips (NOCS), since 2007; IEEE International Conference on Multimedia & Expo (ICME), since 2006; IEEE Workshop on Embedded Computer Systems: Architectures, MOdeling, and Simulation (SAMOS), since 2006; IEEE International Conference on Nano-Networks (Nano-Net), since 2006; IEEE/ACM Design Automation Conference (DAC), since 2005; IEEE International Symposium on Microarchitecture (MICRO), since 2005; IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia), since 2005; IEEE Symposium on Integrated Circuits and Systems Design (SBCCI), since 2005; IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), since 2004; International workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), period 2003 – 2006; IEEE/ACM Design Automation and Test in Europe (DATE) Conference, period 2003 – 2005.

8.5 Keynotes, Tutorials & Seminars

2012 "Towards the Design of Smart Ultra-Low-Power Systems for Wireless Body Sensor Networks", **Keynote Presentation** at the *2012 ICST/IEEE International Body Sensor Networks Conference (BodyNets)*, Oslo, Norway, September 2012.

"Wireless Body Sensor Network (WBSN) Design", **Full-Day Tutorial Organizer and Speaker** at the *17th ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, January 2012.

"System-Level Design and Optimization of Smart and Ultra-low-Power wireless body sensor networks", scheduled **Keynote Presentation** at the *6th IEEE Winter School on Heterogeneous Embedded Systems Design (FETCH 2012: Ecole d'hiver Francophone sur les Technologies de Conception des Systèmes embarqués Hétérogènes)*, Alpe d'Huez, France, January 2012.

"New Modeling Methodologies for Thermal Analysis of 3D ICs and the Advanced Cooling Technologies of the Future", **Half-Day Tutorial Organizer and Speaker** at the *25th International Conference on VLSI Design (VLSIDesign 2012)*, Chennai, India, January 2012.

2011 "Understanding the Impacts of Green Computing on Datacenter Design and Operation", **Keynote Presentation** at the *5th EU Datacenter Dynamics Conference (DATACENTERDYN)*, Lyon, France, November 2011.

"System-Level Thermal-Aware Design of 3D Multi-Processors with Inter-Tier Liquid Cooling", **Keynote Presentation** at the *17th IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Paris, France, September 2011.

"Thermal-Aware System-Level Design of 2D/3D MPSoC Architectures", **Keynote Presentation** at the *23rd IEEE Euromicro Conference on Real-Time Systems (ECRTS)*, Porto, Portugal, July 2011.

"Towards Smart and Energy-Aware Wireless Body Sensor Nodes for Personal Health Monitoring", **Half-Day Invited tutorial Speaker** at the *5th IEEE International Symposium on Medical Information and Communication Technology (ISMICT) Conference*, Montreux, Switzerland, March 2011

"Emerging Thermal-Aware Design Flows and CAD Tools for 3-D Multi-Processor SoCs", **Full-Day Invited Tutorial Organizer and Speaker** at 2011 IEEE/ACM Design Automation and Test in Europe Conference (DATE 2011), France, March 2011.

"System-Level Design and Power Management of Wireless Body Sensor Nodes", **Invited Hot-Topic Seminar** at ST Microelectronics, Agrate, Italy, February 2011.

"Low-Power and Real-Time Biomedical Signals Monitoring", **Invited Talk** at the 5th

IEEE Winter School on Heterogeneous Embedded Systems Design (FETCH 2011), Canada, January 2011.

2010 "Thermal-Aware Design of 3D ICs with Inter-Tier Liquid Cooling", **Invited Talk** at *56th International Electron Devices Meeting (IEDM 2010)*, special session on: "Confluence of Technology and Design – Challenges for Non-Conventional Devices and 3D LSIs", USA, December 2010.

"Manufacturing, CAD and Thermal-Aware Architectures for 3-D MPSoCs", **Invited Tutorial Organizer and Speaker** at *2010 International Conference on Computer-Aided Design (ICCAD 2010)*, USA, November 2010.

"Low-Complexity OS-Based Thermal Modeling and Active Cooling Management in 3D MPSoCs", **Invited Technology Seminar Speaker** at IBM T.J. Watson Research Center, USA, October 2010.

"Thermal-Aware Design of 2D and 3D Multi-Processor System-on-Chip Architectures", **Invited Talk** at the 2010 Summer School of the ARTIST EU Network-of-Excellence on Embedded Systems Design, France, September 2010.

"Thermal Analysis and Thermal-Aware Design of 3D MPSoCs with Active Cooling", **Tutorial Speaker** at *47th Design Automation Conference (DAC 2010)* Full-Day Tutorial: "3D: New Dimensions in IC Design", USA, June 2010.

"Thermal Management in future 3D multiprocessor systems on chip", **Invited Talk** at *47th Design Automation Conference (DAC 2010)* Workshop: "Multiprocessor System on Chip: Programmability, Run-Time Support and Hardware Platforms for High Performance Applications", USA, June 2010.

"Thermal Modeling, Analysis and Management of 2D/3D Multi-Processor System-on-Chip", **Invited Talk** at the *2010 Engineering School on Design of Low-Power and Real-Time Embedded Systems (ECOFAC 2010: Ecole sur la conception faible consommation pour les systèmes embarqués temps reels)*, France, March 2010.

"Green Computing Implies Minimizing Energy Costs and Pollution of Information Technology Systems", **Keynote** at the *14th INFORUM Conference on New Information Technologies*, CERN and Swiss Office for Industrial and Technology Promotion (OPI), March 2010.

"Thermal Modeling and Management for 2D and 3D Multiprocessor System-on-Chip", **Full-Day Tutorial Speaker** in the 23rd *IEEE VLSI Design Conference*, India, January 2010.

"Active Cooling for Thermal Management of 3D MPSoCs", **Invited Talk** at the *4th IEEE Winter School on Heterogeneous Embedded Systems Design (FETCH 2010: Ecole d'hiver Francophone sur les Technologies de Conception des Systèmes embarqués Hétérogènes)*, France, January 2010.

2009 "Thermal Modeling of Active Cooling for 3D MPSoCs", **Invited Talk** at the *9th IEEE International Forum on Embedded MPSoC and Multicore*, USA, August 2009.

"Novel Design Methods for 3D High-Performance Embedded Architectures", **Invited Seminar** at the Computer Science and Engineering School, University of California Santa Cruz (UCSC), USA, August 2009.

"Thermal Modeling and Characterization of 3D Chips", **Half-Day Tutorial Speaker** at the *3rd IEEE System Design for 3D Silicon Integration Workshop (D43D)*, MINATEC-LETI, France, June 2009.

"Thermal-Aware Design of Nano-Scale Multi-Core Architectures", **Invited Keynote** at the *Scientific Day Workshop on Low-Power SoC Design*, Research Group on SoC-SiC Design, National Center of Scientific Research (CNRS), France, May 2009.

"Thermal Modeling, Analysis and Management of Multi-Processor Systems-on-Chip", **Invited Talk** at the Barcelona Supercomputing Center as part of the *Keynote Seminars of the EU FP6 European Network of Excellence on High-Performance Embedded Architectures and Compilers (HiPEAC), European Commission*, Spain,

January 2009.

2008 "Active Thermal Management of 2D/3D Multi-Processor Embedded Architectures", **Invited Talk** at the School of Computer Engineering, KOC University, Turkey, December 2008.

"Thermal Modeling and Management of High-Performance System-on-Chip Platforms", **Invited Talk** at Sun Microsystems Research Center, Santa Clara, USA, November 2008.

"New Exploration Frameworks for Temperature-Aware Design of MPSoCs", **Invited Embedded Tutorial** at the *8th IEEE International Forum on Embedded MPSoC and Multicore*, Germany, July 2008.

2007 "Embedded HW/SW Codesign with Xilinx Virtex-II Pro Board", **Half-Day Tutorial Speaker** at the School of Computer Science, University of Bologna, Italy, October 2007.

"Leakage Management and Thermal Modeling of the Register File of VLIW Architectures", **Invited Talk** in the *1st Workshop CLEAN Integrated Project*, EU FP6 Programme, European Commission, Stresa, Italy, June 2007

2006 "Dynamic Memory Management for Advanced MPSoC", **Invited Talk** at the School of Computer Science, University of Bologna, Italy, October 2006.

"FPGA-Based Emulation Methodologies for Embedded System Optimization", **Invited Talk** at TIMA Labs, Grenoble, Italy, June 2006.

2005 "Design Flows of MPSoCs with FPGA-Based Platforms", **Invited Talk** at the School of Computer Science, University of Bologna, Italy, November 2005.

2004 "How early stage research mobility can change completely your point of view about multicultural research expectations", **Invited Talk** in the conference *Early Stage Researcher Mobility in Europe - Meeting Challenges & Best Practice*, European Commission, Euroscience, Marie Curie Fellowship Association, Lisbon, Portugal, February 2004

"Evolution and Future Perspectives of Young Researchers in the Europe of Knowledge", **Invited Talk** in the conference *The Europe of Knowledge 2020: A Vision for University-Based Research and Innovation*, European Commission, Liege, Belgium, June 2004.

8.6 Teaching in high education institutions

2010-2011 Lecture: Circuits and Systems-I (EPFL), taught in English, B.Sc. level

Lecture+Lab: Microprogrammed Embedded Systems (EPFL), taught in English and French, B.Sc. level. **(New Bachelor Course at SEL-EPFL, evaluation: 5.2/6.0)**

Lecture: Circuits and Systems-I (EPFL), taught in English and French for the Sections of Electrical Engineering (SEL), Communication (SC) and Informatics (SIN), B.Sc. level.

Lecture+Lab: Multi-Processor System-on-Chip Design and Synthesis on FPGAs (EPFL), English course, PhD level. **(New PhD Course at EDEE, evaluation: 5.5/6.0)**

2009-2010 Lecture: Circuits and Systems -I and II (EPFL), taught in English and French for SEL, B.Sc. level.

2008-2009 Lecture: Structure and Technology of Computer Systems (UCM), B.Sc. level.

Lecture: Advanced Computer Architecture (UCM), M.Sc. level.

Lecture+Lab: System-on-Chip Design on FPGAs (UCM), M.Sc. level.

Short course: Multi-Processor System-on-Chip Design (EPFL), PhD level.

2007-2008
Lecture: Advanced Computer Architecture (UCM), M.Sc. level.
Lecture+Lab: Digital Design Methodologies (UCM), B.Sc. level.
Seminars+Lab: Integrated System Design (EPFL), PhD level.
Seminar: Allocation Techniques in Integrated System Design (EPFL), PhD level.

2006-2007
Lecture: Advanced Computer Architecture (UCM), M.Sc. level.
Lecture: Basic Computer Architecture (UCM), B.Sc. level.
Lecture+Lab: Digital Design Methodologies (UCM), PhD level.
Seminars+Lab: Integrated System Design (EPFL), PhD level.

2005-2006
Lecture+Lab: Operating Systems (UCM), B.Sc. level.
Lab: High-Level Synthesis (UCM), PhD level.
Lab: Basic Computer Architecture (UCM), B.Sc. level.
Lecture+Lab: Software Optimization Techniques for Computers (UCM), M.Sc. level
Industrial Course: Linux Security & Advanced Administration (UCM), M.Sc. level.

2004-2005
Lab: Operating Systems (UCM), B.Sc. level.
Lab: Basic Computer Architecture (UCM), B.Sc. level
Lab: High-Level Synthesis (UCM), PhD level.
Lab: Technology of Computers (UCM), M.Sc. level.

2003-2004
Lab: Software Optimization Techniques for Computers (UCM), M.Sc. level.
Lab: Basic Computer Architecture (UCM), B.Sc. level.

2002-2003
Lab: Software Optimization Techniques for Embedded Systems (UCM), M.Sc. level.
Lab: Basic Computer Architecture (UCM), B.Sc. level.

8.7 Ph. D. Students

Director at EPFL
A. Dogan, started March 2009.
H. Mamaghanian, started June 2009
M. Sabry, started October 2009.
A. Sridhar, started January 2010.
S. Raghav, started March 2010.
I. Beretta, started April 2010.
A. Vincenzi, started October 2010.
K. Kanoun, started March 2011.
R. Braojos, started October 2011.

Director at UCM
J.M. Velasco Cabo, PhD granted in April 2010 (*suma cum laude*): "Optimización de la Memoria Virtual En Java" (Directors: Katzalin Olcoz, David Atienza and Francisco Tirado)
P. G. Del Valle, finalization expected in March 2012.

F. Rincon, finalization expected in March 2012.

Advisor at EPFL M.-Haykel Ben Jamaa, September 2009.

F. Zanini, December 2011.

Co-referee C. Poucet, IMEC & K.U. Leuven, expected 2010.

8.8 M.Sc. Students

Director at EPFL H. Samy, "PMSM: Power Management Systems and Monitoring infrastructure for servers and racks of datacenters" (in Cooperation with Credit Suisse IT Datacenter in Lausanne), September 2011.

E. Rincon, "Interface for automatic acquisition and processing of nutritional data and physical sport quality monitoring", June 2010.

R. Braojos, "Removal of Image Artifacts in CMOS Cameras for iPhone 3GS", June 2010.

V. Viswanathan, "Modeling of Liquid Cooling Mechanisms for 3D Chips", September 2009.

C. Seiculescu, "Design Methodologies for Efficient Synthesis of Networks-On-Chip on FPGA Platforms", November 2008.

S.-K. Bobba, "Misalignment-Immune Logic Synthesis Methods for Deep-Sub-Micron CMOS", November 2008.

Director at UCM C. Garcia, "Energy and Performance Impact of Security Inclusion in IEEE 802.15.4 Based Wireless Sensor Networks", September 2009.

V. Barbero, "ECG baseline wander removal and noise suppression analysis in an embedded platform", September 2009.

J. T. Vall-Llovera, "Design and Modeling of an Ultra-Low-Power Synthesizable Processor for Multimedia Embedded Systems", September 2008.

E. Martinez-Pacheco, A. González, F. Navarro, "Hardware/Software Co-Design of Application-Specific Processing Units for Embedded Systems", September 2007.

S. Belmar, C. M. Gonzalez, P. Virsedano, "Optimization of Dynamic Memory Allocation in Embedded Systems Using Evolutionary Computation", Awarded the **IBM Innovative Project Award - V Certamen Arquímedes 2007**, Ministry of Education and Science.

P. G. Del Valle, E. Perez, J. Gomez, "Transparent Monitoring Mechanisms for Multi-Processor Embedded Systems", September 2005.

Director at IMEC B. Veeckmans, "Optimization of a Memory Subsystem of a Turbo Decoder", June 2004.

C. Poucet, "Statistics Extraction Framework of Dynamic Memory Allocators in Low-Power Embedded Systems", September 2004.

9. ADDITIONAL INTERNATIONAL RESEARCH EXPERIENCE

Jun. – Oct. 2004 Invited Researcher in the Network-on-Chip research group at Gates Computer Science Faculty of Stanford University, Palo Alto, CA, USA.

10. SCIENTIFIC PUBLICATIONS (Inverse Chronological Order)

10.1 Patents

1. Francky Catthoor, Mohamed Sabry, Ma Zhe, David Atienza, "Method and System for Real-Time Error Mitigation", US Patent, Deposit nr: 13467758, May 9th, 2012.
2. Federico Angiolini, David Atienza, Giovanni De Micheli, "Method to manage the load of peripheral elements within a multicore system", Granted US Patent nr: US 7,995,599B2, August 9th, 2011.
3. Ahmed Dogan, Jeremy Constantin, Andreas Burg, David Atienza, "Multi-Core Architecture Design for Ultra Low Power Wearable Health Monitoring Systems", US Patent, Deposit nr: P2371PCOP, March 10th, 2012.
4. Juri Ranieri, Alessandro Vincenzi, Amina Chebira, Martin Vetterli, David Atienza "Optimal Thermal Characterization and Minimal Sensor Placement for Multicore Processors Using EigenMaps", US Patent, Deposit Nr.: P2350US0P, December 13th, 2011.
5. Hossein Mamaghanian, Francisco Rincón Vallejos, Nadia Khaled, David Atienza, Pierre Vandergheynst, "Automatic online delineation of a multi-lead electrocardiogram bio signal", US Patent, Deposit nr: P2208PC00/0013-155, December 2010.

10.2 Books

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3. Vincenzo Rana, David Atienza, Marco Domenico Santambrogio, Donatella Sciuto, "A Reconfigurable Network-on-Chip Architecture for Optimal Multi-Processor SoC Communication", in the book "*VLSI-SOC: Design Methodologies for SoC and SiP*", Springer, Dordrecht/London/Boston, Ed. Soudris, Piguet Reis, Ch. 13, pp. 232-250 , March 2010.
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C3. Arvind Sridhar, Mohamed Sabry, David Atienza, "Thermal Balancing of Liquid-Cooled 3D MPSoCs Using Channel Modulation", *Proc. of Design, Automation and Test in Europe (DATE '12)*, ACM and IEEE Press, Dresden, Germany, March 2012.

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